CLAIMS

1. A method for fabricating semiconductor packages, the method comprising:

providing a circuit board strip including a plurality of unit circuit boards, each unit circuit board having a plurality of first ball lands formed at a first major surface thereof, a plurality of bond fingers formed at an opposite second major surface thereof, vias through the circuit board each electrically connected between a bond finger and a first ball land, and a through hole between the first and second major surfaces;

receiving in each through hole a semiconductor chip having a first major surface, and an opposite second major surface provided with a plurality of input/output pads thereon, wherein the second major surface of the chip faces in the same direction as the first major surface of the respective circuit board;

electrically connecting the input/output pads of each semiconductor chip with associated ones of the bond fingers of the respective circuit board;

encapsulating the semiconductor chips, and filling the through hole of each unit circuit board of the circuit board strip using an encapsulating material;

fusing conductive balls on the first ball lands of each unit circuit board;

singulating the circuit board strip into semiconductor packages respectively corresponding to the unit circuit boards.

2. The method of claim 1, wherein the circuit board strip comprises:

a main strip including a resin substrate having a substantially rectangular strip shape, a first major surface and a second major surface;

a plurality of main slots extending to a desired length in a direction transverse to a longitudinal direction of the main strip while being uniformly spaced apart from one another in the longitudinal direction of the main strip, thereby dividing the main strip into a plurality of sub-strips aligned together in the longitudinal direction of the main strip;

a plurality of sub slots extending to a desired length and serving to divide each of the sub-strips into a plurality of strip portions arranged in a matrix array, each of the strip portions corresponding to one of the unit circuit boards having one of the through holes;

a plurality of first circuit patterns each formed on the first major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the first ball lands;

a plurality of second circuit patterns each formed on the second major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the bond fingers; and

cover coats respectively coated over the first and second major surfaces of the resin substrate while allowing the bond fingers and the ball lands to be exposed therethrough.

3. The method of claim 1, wherein the circuit board strip comprises:

a resin substrate having a substantially rectangular strip shape provided with a first major surface and a second major surface;

a plurality of slots extending to a desired length and serving to divide each of the resin substrate into a plurality of substrate portions arranged in a matrix array, each of the substrate portions corresponding to one of the unit circuit boards having one of the through holes;

a plurality of first circuit patterns each formed on the first major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the first ball lands;

a plurality of second circuit patterns each formed on the second major surface of the resin substrate for an associated one of the strip portions and provided with associated ones of the bond fingers; and

cover coats respectively coated over the first and second major surfaces of the resin substrate while allowing the bond fingers and the ball lands to be exposed therethrough.

4. The method of claim 1, further comprising attaching one or more closure members to the first surface of the substrate strip so that each through hole is covered thereby prior to receiving the semiconductor chip in the respective through hole.

5. The method of claim 2, further comprising:

attaching a plurality of closure members to the first major surface of the circuit board strip in such a fashion that the closure members simultaneously cover associated ones of the through holes, prior to the step of receiving the semiconductor chips in the through holes.

6. The method according to claim 3, further comprising the step of:

attaching a plurality of closure members to the first major surface of the circuit board strip in such a fashion that the closure members simultaneously cover associated ones of the through holes, prior to the step of receiving the semiconductor chips in the through holes.

7. The method according to claim 5, wherein attaching the closure member comprises:

preparing closure member strips each having closure members for an associated one of the sub-strips; and

individually attaching the closure member strips to the sub-strips, respectively, in such a fashion that each of the closure member strips is arranged to cover the main slot formed at one side of an associated one of the sub-strips.

8. The method according to claim 5, wherein attaching the closure member comprises:

preparing a single closure member strip having closure members for all sub-strips of the circuit board strip while having small singulation apertures at a region corresponding

to each of the main slots; and

attaching the closure member strip to the main strip in such a fashion that the closure member strip is arranged to allow each of the small singulation apertures to be aligned with an associated one of the main slots.

9. The method of claim 4, wherein the one or more closure members are removed after encapsulating the semiconductor chips.

10. The method of claim 5, wherein the closure members are removed after encapsulating the semiconductor chips.

11. The method of claim 6, wherein the closure members are removed after encapsulating the semiconductor chips.

12. The method of claim 7, wherein the closure members are removed after encapsulating the semiconductor chips by inserting a bar into one or more of the main slots in a direction from the second major surface of the circuit board strip to the first major surface of the second board strip, thereby detaching an associated one of the closure members from the circuit board strip at one side of the associated closure member.

13. The method of claim 8, wherein the closure members are removed after encapsulating the semiconductor chips by inserting a bar into one or more of the main slots in a direction from the second major surface of the circuit board strip to the first major surface of the second board strip, thereby detaching an associated one of the closure members from the circuit board strip at one side of the associated closure member.

14. The method of to claim 4, wherein each closure member is selected from the group consisting of an insulating tape, an ultraviolet tape, and a copper layer.

15. The method of claim 5, wherein each of the closure members is selected from the group consisting of an insulating tape, an ultraviolet tape, and a copper layer.

16. The method of claim 6, wherein each of the closure members is selected from the group consisting of an insulating tape, an ultraviolet tape, and a copper layer.

17. The method of claim 4, wherein a unitary body of encapsulant material covers the second major surface of all of the unit circuit boards of the circuit board strip.

18. The method according to claim 5, wherein a unitary body of encapsulant material covers the second major surface of all of the unit circuit boards of the circuit board strip.

19. The method according to claim 6, wherein a unitary body of encapsulant material covers the second major surface all of the unit circuit boards of the circuit board strip.

20. The method according to claim 17, wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split.

21. The method according to claim 18, wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split.

22. The method according to claim 19, wherein singulating the circuit board strip is carried out in such a fashion that the encapsulant material and the circuit board strip are simultaneously split.

23. The method of claim 1, wherein encapsulating the circuit board strip comprises:

interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity; and

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface.

24. The method of claim 2, wherein the encapsulating the circuit board strip comprises:

interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity; and

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface.

25. The method of claim 4, wherein the encapsulating the circuit board strip comprises:

interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate

into the cavity; and

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface, fills the through hole, and contacts the closure member.

26. The method of claim 9, wherein the encapsulating the circuit board strip comprises:

interposing the circuit board strip between a pair of mold dies, one of which has cavities and gates, in such a fashion that the second major surface of each of the semiconductor chips faces an associated cavity and a gate into the cavity; and

injecting the encapsulating material into each of the cavities through the associated gate in such a fashion that it flows outwardly from a central portion of the second major surface of the associated semiconductor chip along the second major surface, fills the through hole, and contacts the closure member.

27. The method of claim 1, wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof.

28. The method of claim 2, wherein each unit circuit board of the circuit board strip is further provided with a

plurality of second ball lands at the second major surface thereof.

29. The method of claim 3, wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof.

30. The method of claim 27, further comprising fusing a plurality of conductive balls on the second ball lands.

31. The method of claim 28, further comprising fusing a plurality of conductive balls on the second ball lands.

32. The method of claim 29, further comprising fusing a plurality of conductive balls on the second ball lands.

33. The method of claim 4, wherein each unit circuit board of the circuit board strip is further provided with a plurality of second ball lands at the second major surface thereof.

34. The method of claim 33, wherein the one or more closure members are removed after encapsulating the semiconductor chips.

35. The method of claim 34, further comprising fusing a plurality of conductive balls on the second ball lands.